AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated hereafter.

Claims:

1. (Currently Amended) A system for testing an abstracted timing model representative of an integrated circuit design comprising:

a controller;

memory associated with said controller for storing electronic format instructions;

said controller is configured to:

receive a reference timing value representative of a time required for a signal to propagate through a path represented by a first model of a circuit;

receive an extracted model timing value representative of a time required for a signal to propagate through a path represented by a second model of the circuit, wherein the second model is an abstraction of the first model;

determine a difference between said reference timing value and said extracted model timing value;

determine whether said difference is within a predetermined permissible range; and

output an indication of success if said difference falls within said predetermined permissible range.

2. (Previously Presented) The system of claim 1, wherein said memory is further configured to store data representing said predetermined permissible range.

3. (Previously Presented) The system of claim 1, wherein said controller is configured in accordance with said electronic format instructions stored on said memory.

4. (Previously Presented) The system of claim 1, wherein said controller is further configured to generate the first model.

5. (Cancelled)

6. (Cancelled)

7. (Previously Presented) The system of claim 1, wherein said controller is further configured to generate said reference timing value.

8. (Previously Presented) The system of claim 7, wherein said controller is further configured to generate said extracted model timing value.

9. (Cancelled)

10. (Currently Amended) The system of claim 1 ~~6~~, wherein said controller is further configured to generate said second model.

11. (Currently Amended) A method of testing an abstracted timing model, comprising the steps of:

receiving a reference timing value representative of a time required for a signal to propagate through a path represented by a first model of a circuit;

receiving an extracted model timing value representative of a time required for a signal to propagate through a path represented by a second model of the circuit, wherein the second model is an abstraction of the first model;

determining ~~the~~ a difference between said reference timing value and said extracted model timing value;

determining whether said difference is within a predetermined permissible range; and

outputting an indication of success if said difference falls within said predetermined permissible range.

12. (Cancelled)

13. (Cancelled)

14. (Currently Amended) The method of claim 11 ~~12~~, further comprising the step of generating said first model.

15. (Currently Amended) The method of claim 11 ~~13~~, further comprising the step of generating said second model.

16. (Currently Amended) A computer program for testing an abstracted timing model, the computer program comprising:

a first code segment for receiving a reference timing value representative of a time required for a signal to propagate through a path represented by a first model of a circuit;

a second code segment for receiving an extracted model timing value representative of a time required for a signal to propagate through a path represented by a second model of the circuit, wherein the second model is an abstraction of the first model;

a third code segment for determining ~~the~~ a difference between said reference timing value and said extracted model timing value; and

a fourth code segment for outputting an indication of success if said difference falls within ~~said~~ a predetermined permissible range.

17. (Cancelled)

18. (Cancelled)

19. (Currently Amended) A computer program according to claim 16 ~~17~~, further comprising a sixth code segment for generating said first model.

20. (Currently Amended) A computer program according to claim 16 ~~18~~, further comprising a sixth code segment for generating said second model.

21. (Previously Presented) A method for testing an abstracted timing model, comprising the steps of:

comparing a first value that is responsive to a time required for a signal to propagate through a path represented by a first model of a circuit with a second value that is responsive to a time required for a signal to propagate through a path represented by a second model of the circuit, wherein the second model is an abstraction of the first model; and

outputting a result of the step of comparing the first value and the second value.

22. (Previously Presented) The method of claim 21, wherein the result identifies a difference between the first and second values.

23. (Previously Presented) The method of claim 21, wherein the result indicates whether a difference between the first and second values exceeds a pre-determined threshold.

24. (Previously Presented) A system for testing an abstracted timing model, comprising:

means for comparing a first value that is responsive to a time required for a signal to propagate through a path represented by a first model of a circuit with a second value that is responsive to a time required for a signal to propagate through a path represented by a second model of the circuit, wherein the second model is an abstraction of the first model; and

means for outputting a result of the step of comparing the first value and the second value.

25. (Previously Presented) The system of claim 24, wherein the result identifies a difference between the first and second values.

26. (Previously Presented) The system of claim 24, wherein the result indicates whether a difference between the first and second values exceeds a pre-determined threshold.